HARRIS SEMICONDUCTOR

DG401, DG403, DG405

July 1995

Monolithic CMOS Analog Switches

Features

- **ON-Resistance <35Ω**
- **Low Power Consumption (P_D <35μW)**
- **Fast Switching Action**
  - **t_{ON} <150ns**
  - **t_{OFF} <100ns**
- **Low Charge Injection**
- **DG401 Dual SPST; Same Pinout as HI-5041**
- **DG403 Dual SPDT; DG190, IH5043, IH5151, HI-5051**
- **DG405 Dual DPST; DG184, HI-5045, IH5145**
- **TTL, CMOS Compatible**
- **Single or Split Supply Operation**

Applications

- **Audio Switching**
- **Battery Operated Systems**
- **Data Acquisition**
- **Hi-Rel Systems**
- **Sample and Hold Circuits**
- **Communication Systems**
- **Automatic Test Equipment**

Description

The DG401, DG403 and DG405 monolithic CMOS analog switches have TTL and CMOS compatible digital inputs.

These switches feature low analog ON resistance (<35Ω) and fast switch time (t_{ON} < 150ns). Low charge injection simplifies sample and hold applications.

The improvements in the DG401/403/405 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±17V.

The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±15V analog input range. The three different devices provide the equivalent of two SPST (DG401), two SPDT (DG403) or two DPST (DG405) relay switch contacts with CMOS or TTL level activation. The pinout is similar, permitting a standard layout to be used, choosing the switch function as needed.

Ordering Information

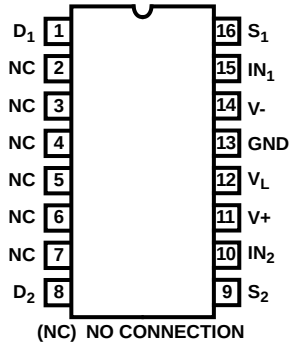
PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG401AK/883 (Note 2)	-55°C to +125°C	16 Lead CerDIP
DG401DJ	-40°C to +85°C	16 Lead Plastic DIP
DG401DY	-40°C to +85°C	16 Lead Plastic SOIC (N)
DG401EJ (Note 1)	-40°C to +85°C	16 Lead Plastic DIP
DG401EY (Note 1)	-40°C to +85°C	16 Lead Plastic SOIC (N)
DG403AK/883 (Note 2)	-55°C to +125°C	16 Lead CerDIP DIP
DG403DJ	-40°C to +85°C	16 Lead Plastic DIP
DG403DY	-40°C to +85°C	16 Lead Plastic SOIC (N)
DG403EJ (Note 1)	-40°C to +85°C	16 Lead Plastic DIP
DG403EY (Note 1)	-40°C to +85°C	16 Lead Plastic SOIC (N)
DG405AK/883 (Note 2)	-55°C to +125°C	16 Lead CerDIP
DG405DJ	-40°C to +85°C	16 Lead Plastic DIP
DG405DY	-40°C to +85°C	16 Lead Plastic SOIC (N)
DG405EJ (Note 1)	-40°C to +85°C	16 Lead Plastic DIP
DG405EY (Note 1)	-40°C to +85°C	16 Lead Plastic SOIC (N)

NOTES:

1. Extended Processing Flow.
2. Refer to Military data sheet for complete specifications.

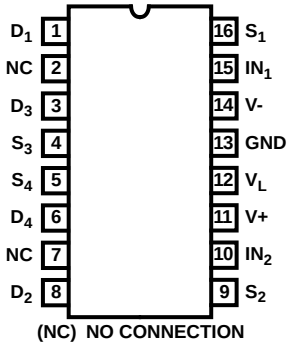
Pinouts

DG401 (CDIP, PDIP, SOIC)
TOP VIEW



(NC) NO CONNECTION

DG403, DG405 (CDIP, PDIP, SOIC)
TOP VIEW

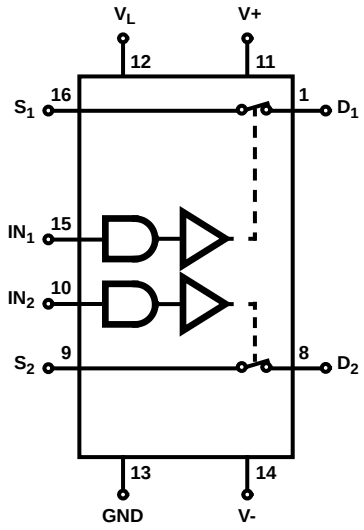


(NC) NO CONNECTION

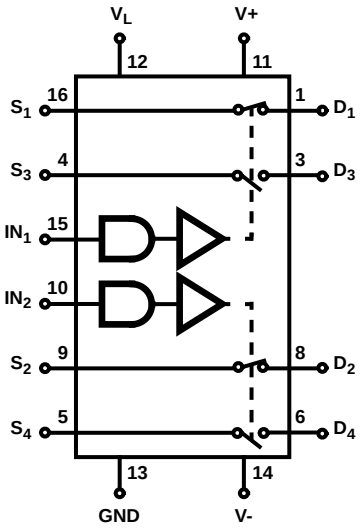
File Number **3284.4**

Functional Diagram

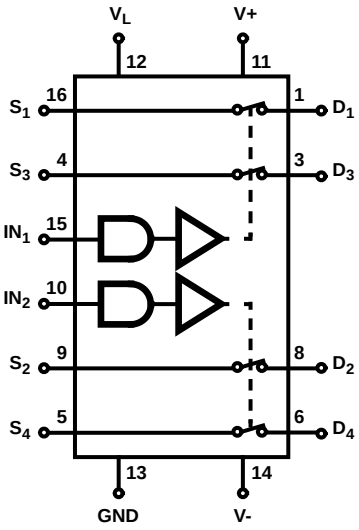
DG401



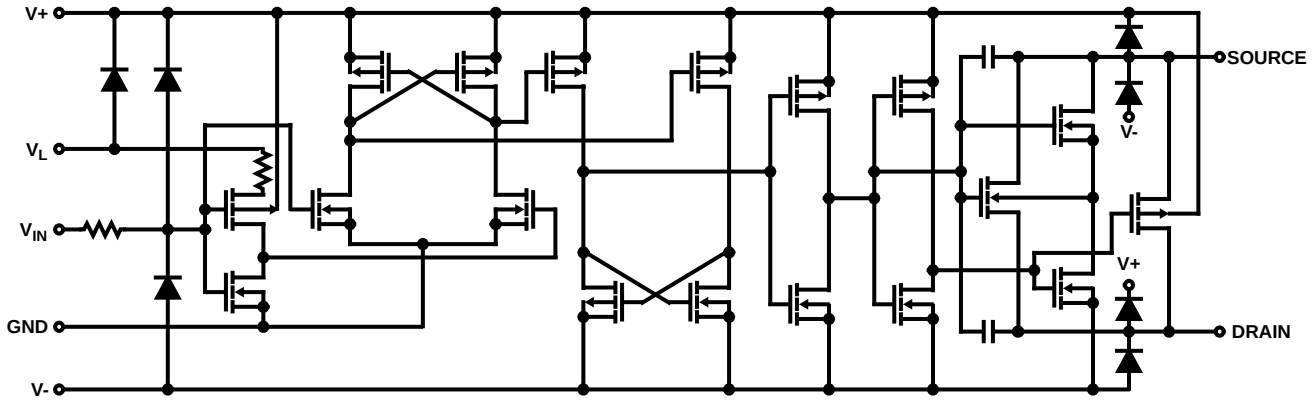
DG403



DG405



Schematic Diagram



Truth Table

LOGIC	DG401	DG403		DG405
	SWITCH	SWITCH 1, 2	SWITCH 3, 4	SWITCH
0	OFF	OFF	ON	OFF
1	ON	ON	OFF	ON

NOTE: Logic “0” ≤0.8V. Logic “1” ≥2.4V.

Absolute Maximum Ratings

V+ to V- . . . . . +44.0V
GND to V- 25V
VL . . . . . (GND - 0.3V) to (VC+) +0.3V
Digital Inputs (Note 1), V_S, V_D . . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous (Any Terminal) Current, (Note 1) . . . . . ±30mA
Peak Current, S or D (Note 1) . . . . . ±100mA (Pulsed 1ms, 10% Duty Cycle)
Storage Temperature Range (D and E Suffix) . . . . -65^oC to $+125^oC$

Thermal Information

Thermal Resistance (Note 2) θ_{JA}
Plastic DIP Package . . . . . $90^oC/W$
SOIC Package . . . . . $115^oC/W$
Lead Temperature (Soldering 10s) . . . . . $+300^oC$ (SOIC - Lead Tips Only)
Operating Temperature (D and E Suffix) . . . . . -40^oC to $+85^oC$
Junction Temperature (PDIP, SOIC) . . . . . $+150^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . ±20V Max
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Input Low Voltage . . . . . 0.8V Max
Input High Voltage . . . . . 2.4V Min
Input Rise and Fall Time 20ns

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, V_L = 5V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITION	(NOTE 4) TEMP	D SUFFIX -40°C TO +85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 300Ω, C_L = 35pF	Room	-	100	150	ns
Turn-OFF Time, t_{OFF}		Room	-	60	100	ns
Break-Before-Make, Time Delay (DG403), t_D	R_L = 300Ω, C_L = 35pF	Room	5	12	-	ns
Charge Injection, Q	C_L = 10,000pF, V_{GEN} = 0V, R_{GEN} = 0Ω	Room	-	60	-	pC
OFF Isolation Reject Ratio, OIRR	R_L = 100Ω, C_L = 5pF, f = 1MHz	Room	-	72	-	dB
Crosstalk (Channel-to-Channel), CCRR	R_L = 100Ω, C_L = 5pF, f = 1MHz	Room	-	90	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz, V_S = 0V	Room	-	12	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	f = 1MHz, V_S = 0V	Room	-	12	-	pF
Channel ON Capacitance, $C_{D(ON)}$ + $C_{S(ON)}$	f = 1MHz, V_S = 0V	Room	-	39	-	pF
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, I_S = -10mA, V_D = ±10V	Room	-	20	45	Ω
		Full	-	-	55	Ω
Drain-Source ON Resistance, $\Delta r_{DS(ON)}$	V+ = 16.5V, V- = -16.5V, I_S = -10mA, V_D = 5, 0, -5V	Room	-	3	3	Ω
		Full	-	-	5	Ω
Switch OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5 V_D = ±15.5V, V_S = ∓15.5V	Room	-0.5	-0.01	0.5	nA
		Full	-5	-	5	nA
Switch OFF Leakage Current, $I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	Room	-0.5	-0.01	0.5	nA
		Full	-5	-	5	nA
Channel ON Leakage Current, $I_{D(ON)}$	V± = ±16.5V, V_D = V_S = ±15.5V	Room	-1	-0.04	1	nA
		Full	-10	-	10	nA

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, V_L = 5V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	(NOTE 4) TEMP	D SUFFIX -40°C TO +85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DIGITAL CONTROL						
Input Current with V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-1	0.005	1	µA
Input Current with V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-1	0.005	1	µA
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	Room	-	0.01	1	µA
		Full	-	-	5	µA
Negative Supply Current, I-		Room	-1	-0.01	-	µA
		Full	-5	-	-	µA
Logic Supply Current, I_L		Room	-	0.01	1	µA
		Full	-	-	5	µA
Ground Current, I_{GND}		Room	-1	-0.01	-	µA
		Full	-5	-	-	µA

NOTES:

1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. All leads soldered to PC Board.
3. V_{IN} = input voltage to perform proper function.
4. Hot = as determined by the operating temperature suffix.
5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
7. Guaranteed by design, not subject to production test.

Typical Performance Curves

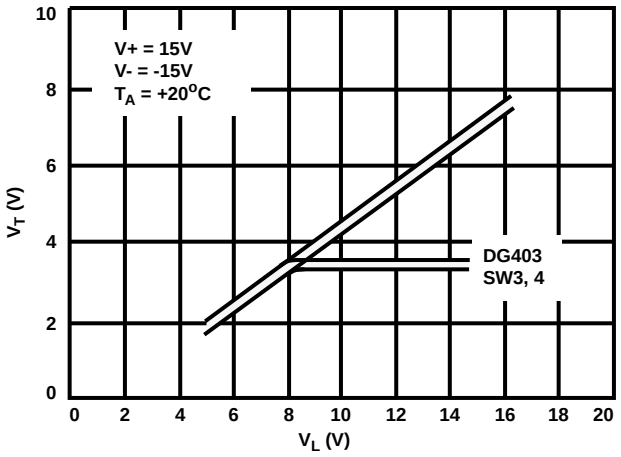


FIGURE 1. INPUT SWITCHING THRESHOLD vs LOGIC SUPPLY VOLTAGE

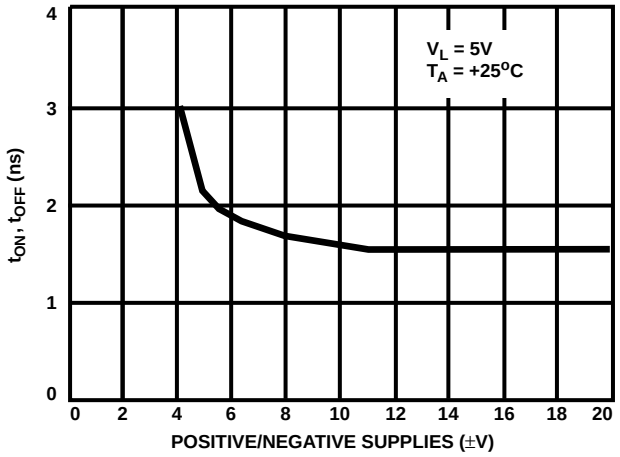


FIGURE 2. INPUT SWITCHING THRESHOLD vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

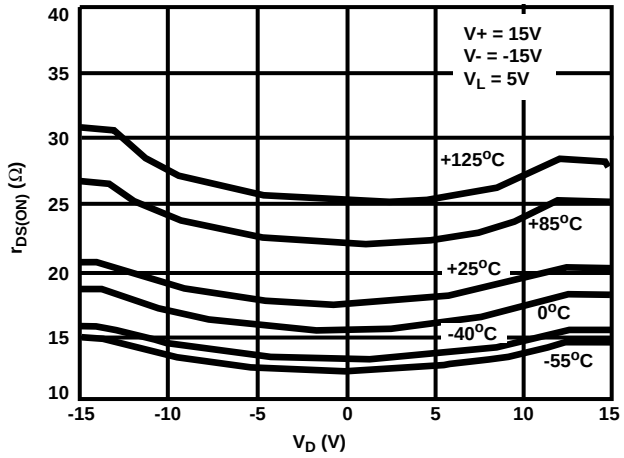


FIGURE 3. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

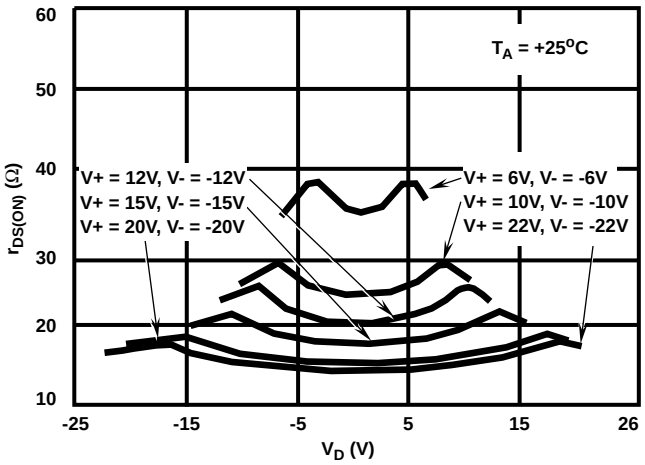


FIGURE 4. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

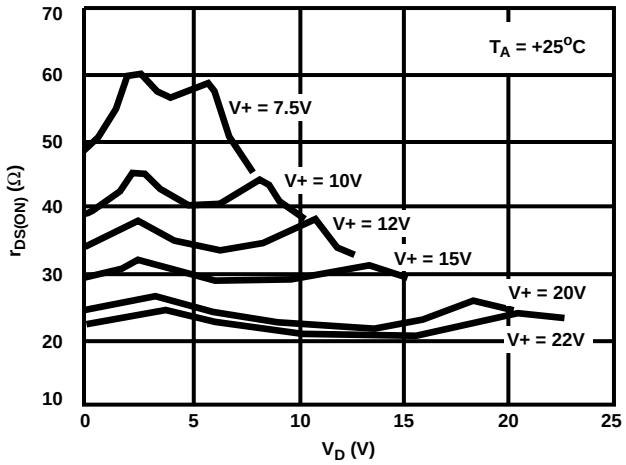


FIGURE 5. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE, V- = -0V

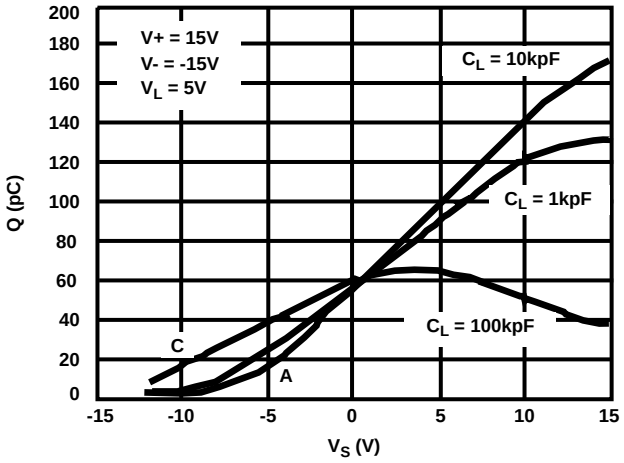


FIGURE 6. CHARGE INJECTION vs ANALOG VOLTAGE (V_S)

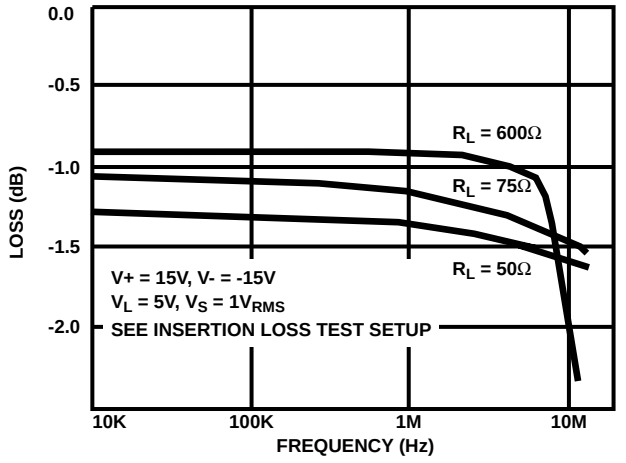


FIGURE 7. INSERTION LOSS vs FREQUENCY

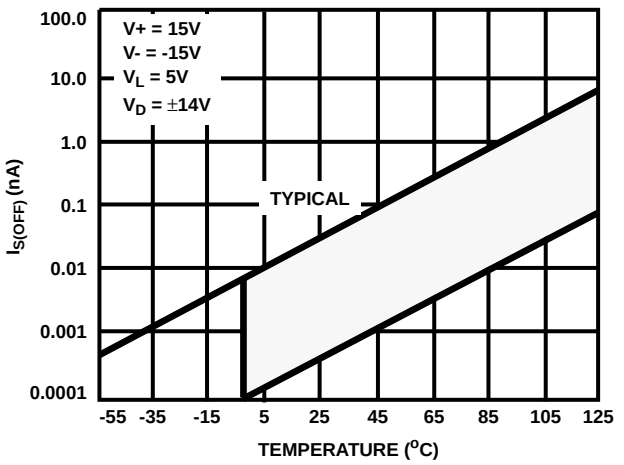


FIGURE 8. $I_{S(OFF)}$ vs TEMPERATURE

Typical Performance Curves (Continued)

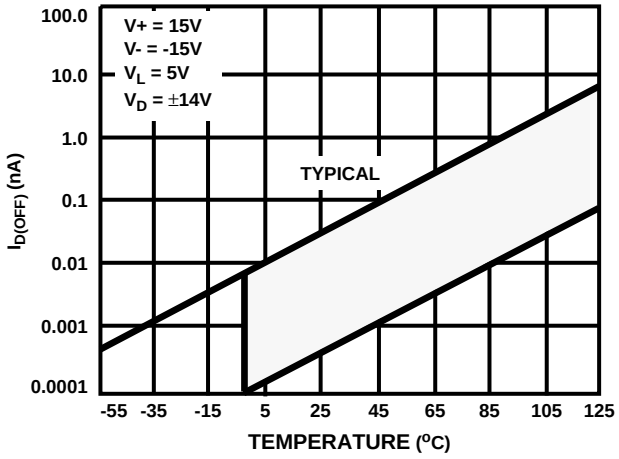


FIGURE 9. $I_{D(OFF)}$ vs TEMPERATURE

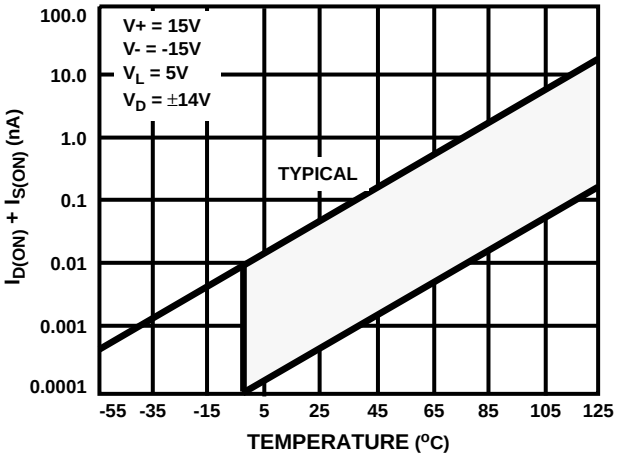


FIGURE 10. $I_{D(ON)} + I_{S(ON)}$ vs TEMPERATURE

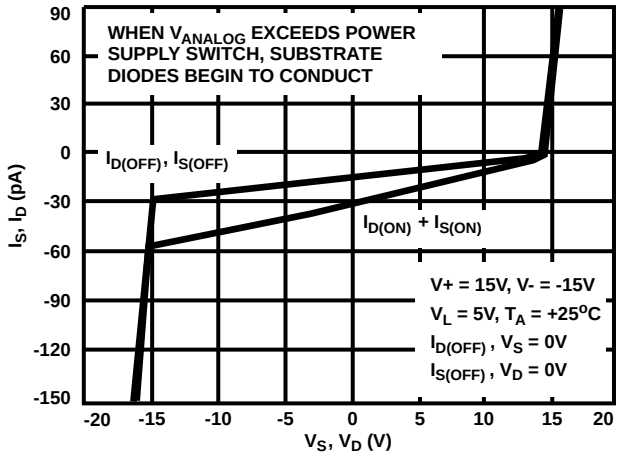


FIGURE 11. LEAKAGE CURRENT vs ANALOG VOLTAGE

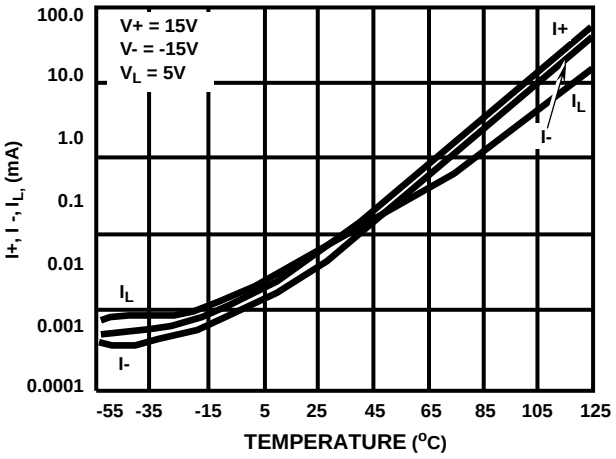


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

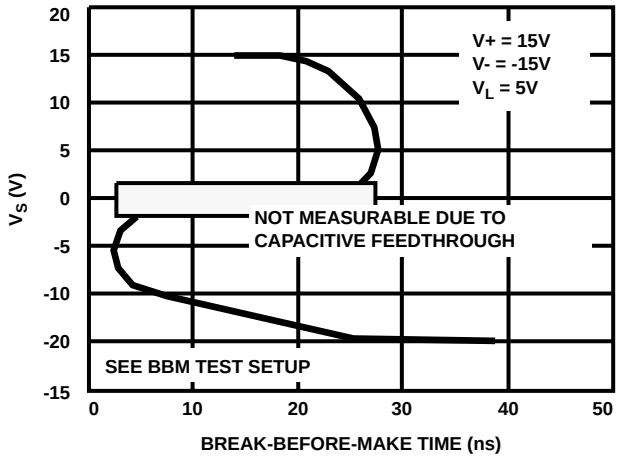


FIGURE 13. BREAK-BEFORE-MAKE vs ANALOG VOLTAGE

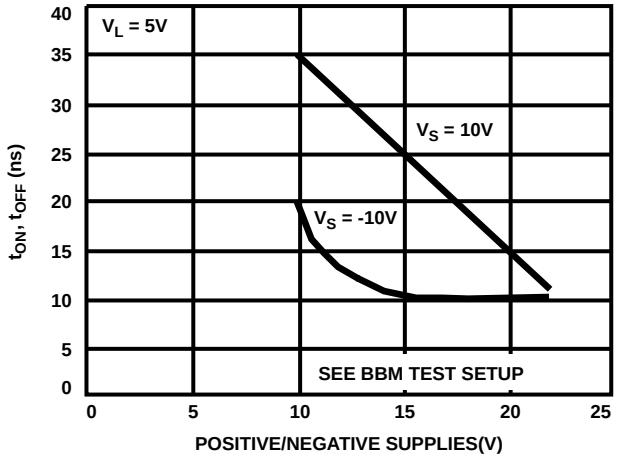


FIGURE 14. BREAK-BEFORE-MAKE vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

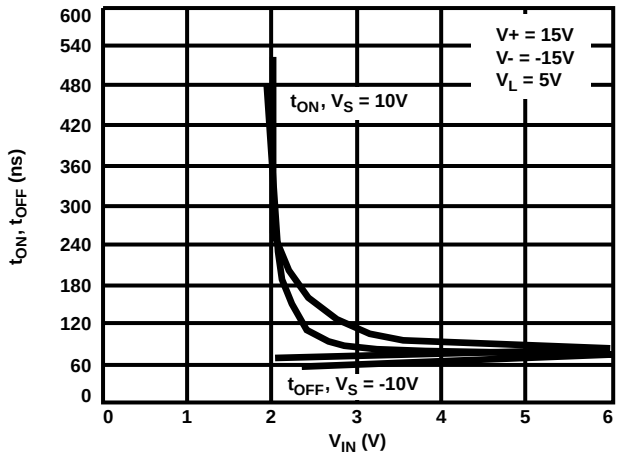


FIGURE 15. SWITCHING TIME vs INPUT LOGIC VOLTAGE (V_{IN}) (NOTE 1)

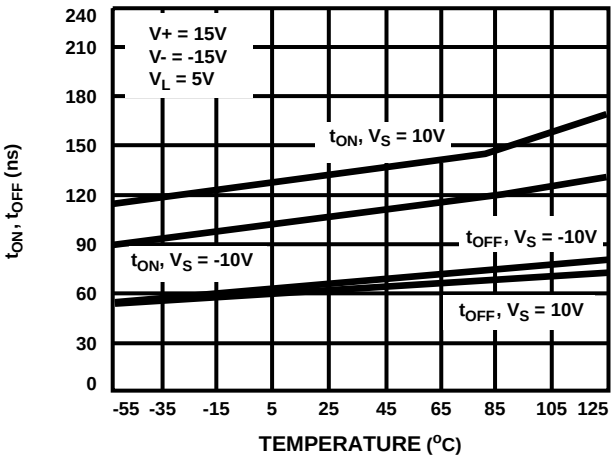


FIGURE 16. SWITCHING TIME vs TEMPERATURE (NOTE 1)

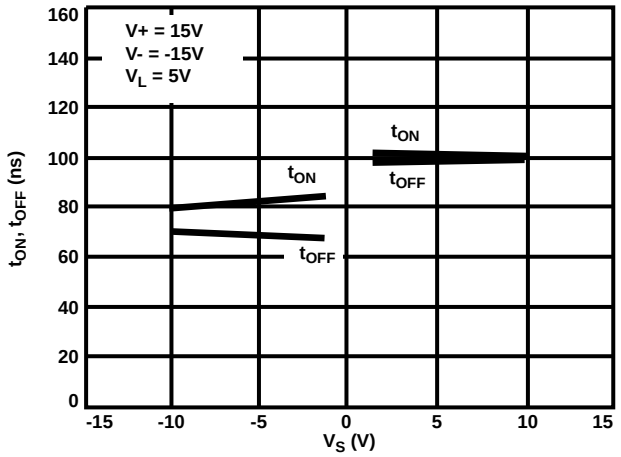


FIGURE 17. SWITCHING TIME vs ANALOG VOLTAGE (NOTE 1)

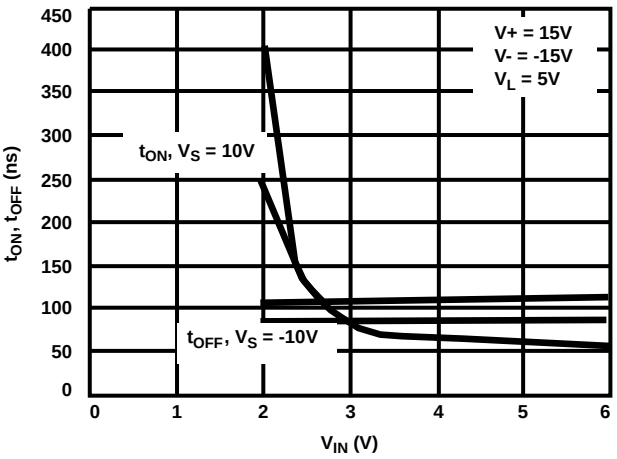


FIGURE 18. SWITCHING TIME vs INPUT LOGIC VOLTAGE (V_{IN}) (NOTE 1)

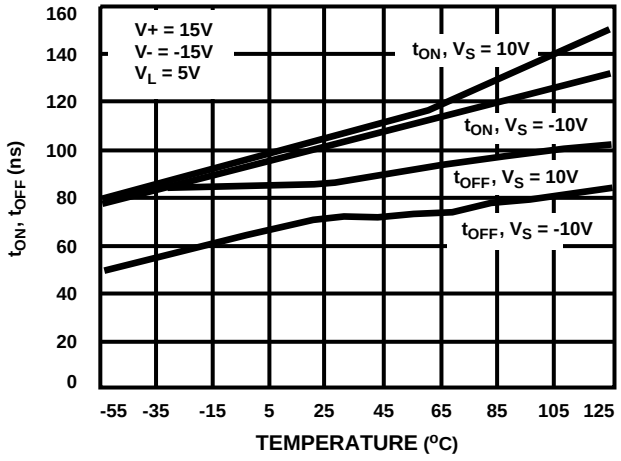


FIGURE 19. SWITCHING TIME vs TEMPERATURE (NOTE 1)

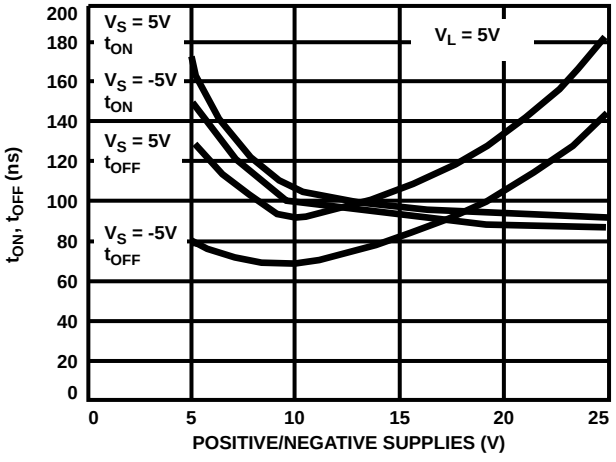


FIGURE 20. SWITCHING TIME vs POWER SUPPLY VOLTAGE (NOTE 1)

Typical Performance Curves (Continued)

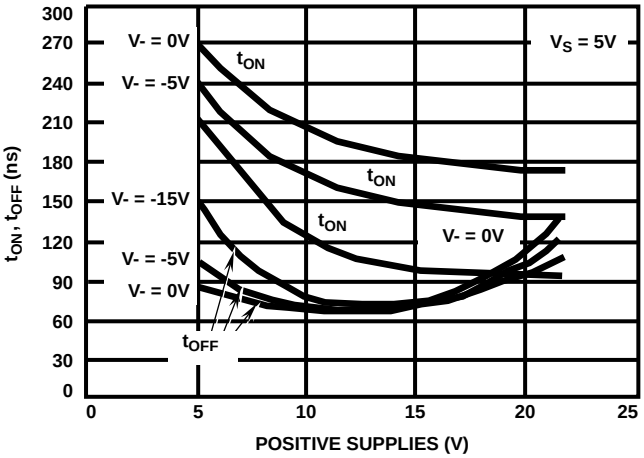


FIGURE 21. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

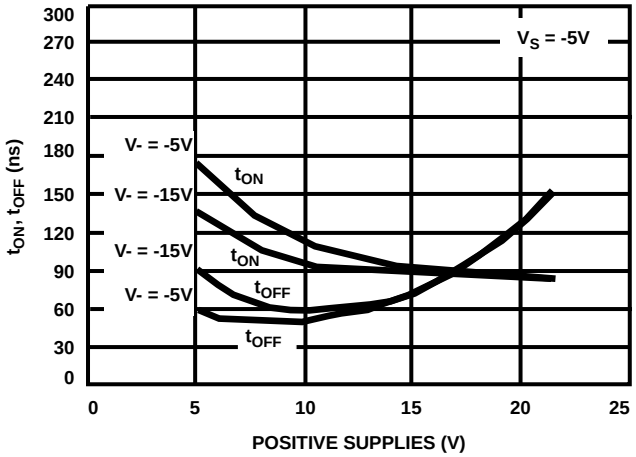


FIGURE 22. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

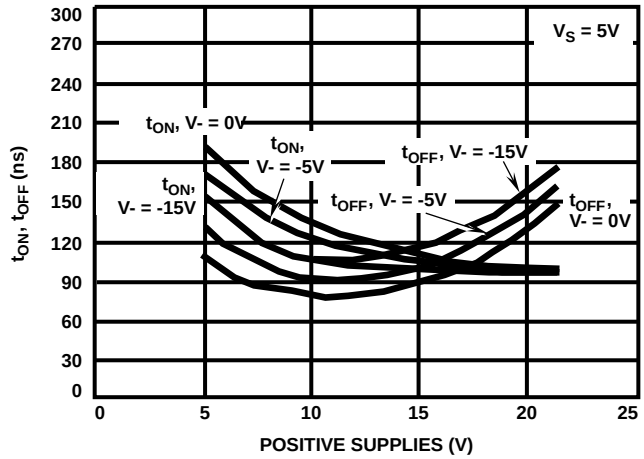


FIGURE 23. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

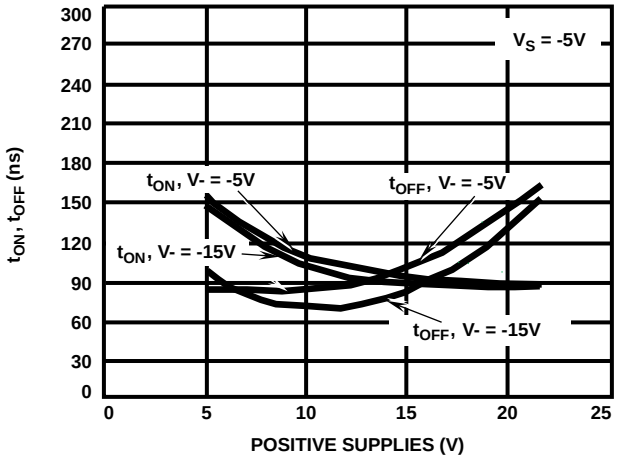
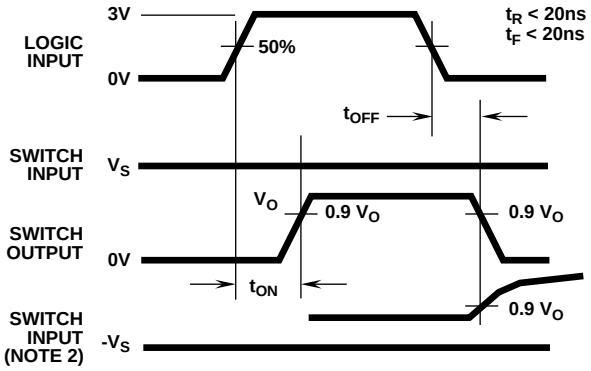


FIGURE 24. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

NOTE:

1. Refer to Figure 1 for test conditions.

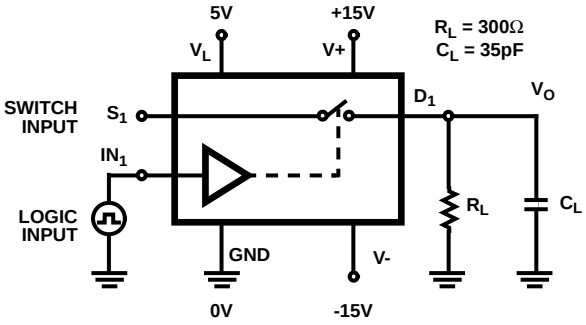
Test Circuits



NOTES:

1. Logic input waveform is inverted for switches that have the opposite logic sense.
2. V_S = 10V for t_{ON}, V_S = -10V for t_{OFF}.

FIGURE 25A.

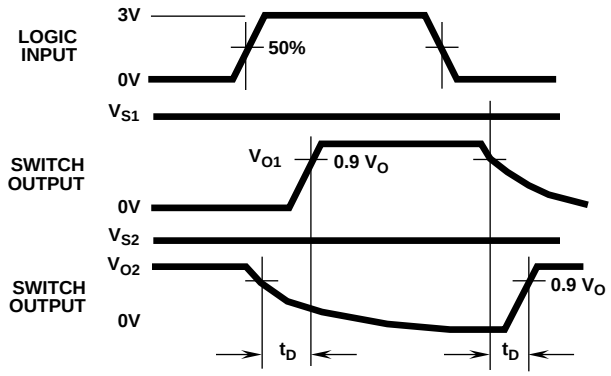


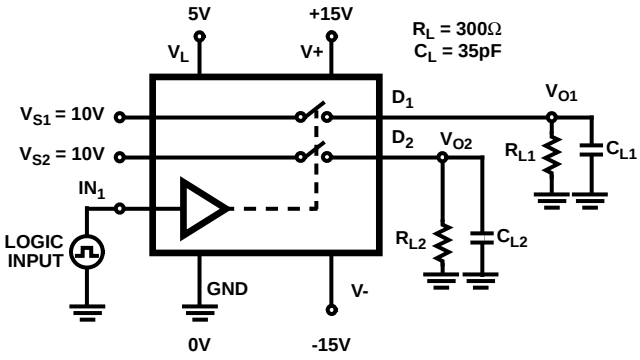
Repeat test for IN_2 and S_2
For load conditions, see Specifications. C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 25B.

FIGURE 25. SWITCHING TIME



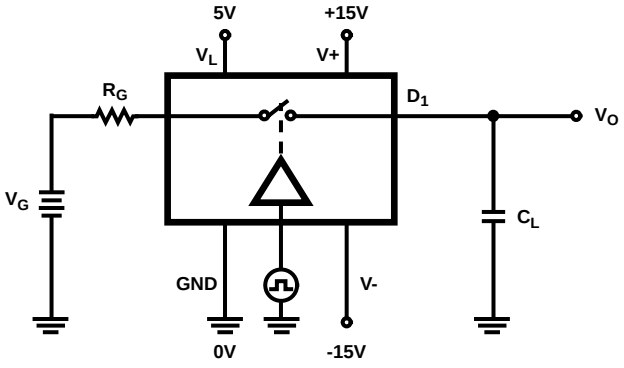


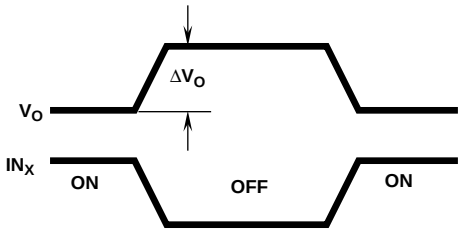
C_L (includes fixture and stray capacitance)

FIGURE 26A.

FIGURE 26B.

FIGURE 26. BREAK-BEFORE-MAKE





$Q = \Delta V_O \times C_L$

FIGURE 27A.

FIGURE 27B.

FIGURE 27. CHARGE INJECTION

Test Circuits (Continued)

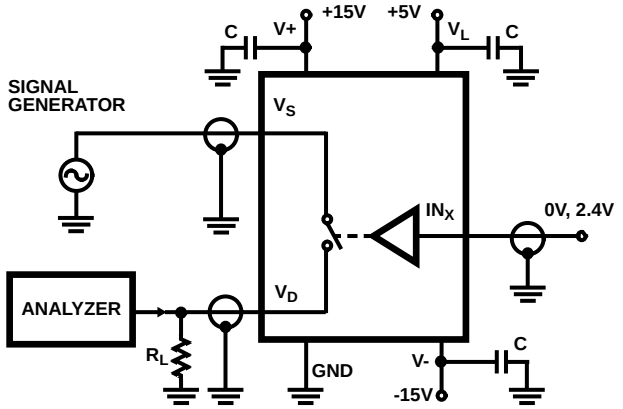


FIGURE 28. OFF ISOLATION

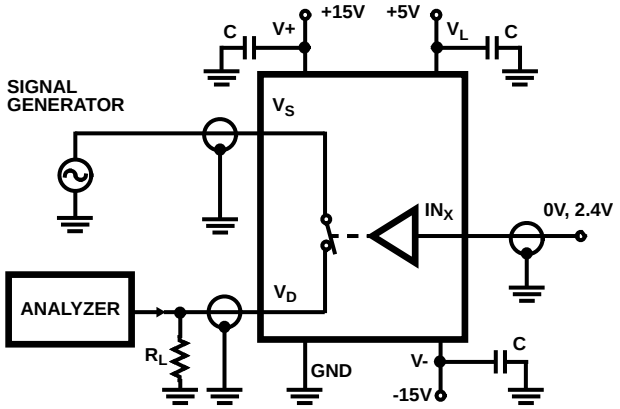


FIGURE 29. INSERTION LOSS

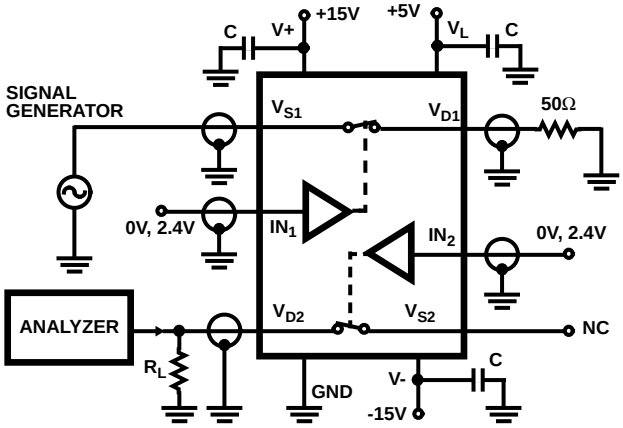


FIGURE 30. CROSSTALK

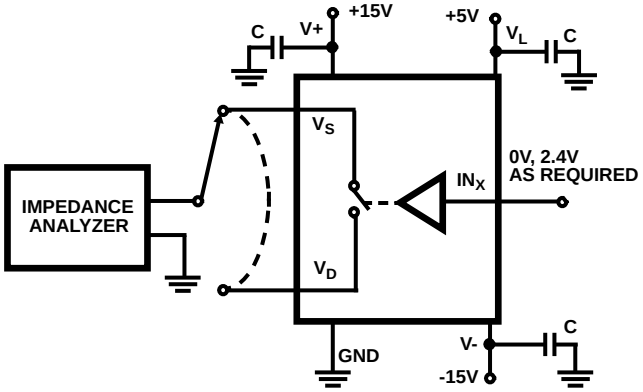


FIGURE 31. CAPACITANCES

Dual Slope Integrators

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2. Another one selects e_{IN} or discharges the capacitor in preparation for the next integration cycle.

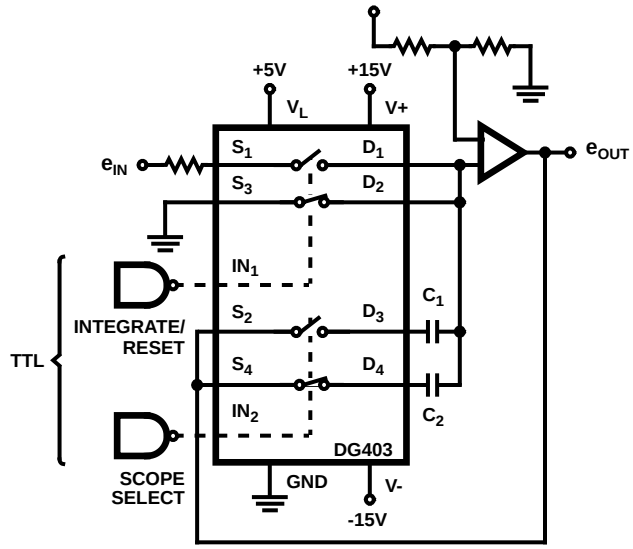


FIGURE 32. DUAL SLOPE INTEGRATOR

Peak Detector

A_3 acting as a comparator provides the logic drive for operating SW_1. the output of A_2 is fed back to A_3 and compared to the analog input e_{IN}. If $e_{IN} > e_{OUT}$ the output of A_3 is high keeping SW_1 closed. This allows C_1 to charge up to the analog input voltage. When e_{IN} goes below e_{OUT} of A_3 goes negative, turning SW_1 off. the system will therefore store the most positive analog input experienced.

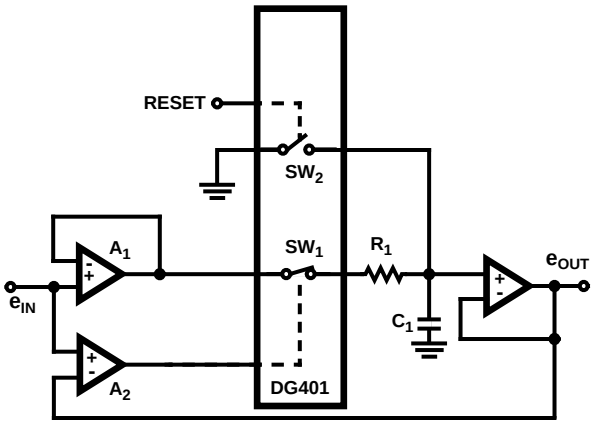


FIGURE 33. POSITIVE PEAK DETECTOR